Remarks/Arguments

Claims 1-20 remain in this application.

The examiner has rejected claims 1-7, 9-11 and 18-20 under 35 USC 102() as being anticipated by *Maeng, et al.* (United States Patent 6,287,878).

The examiner has rejected claims 8 and 12-17 under 35 USC 103(a) as being unpatentable over *Maeng, et al.*, in view of *Kiyokawa, et al.* (United States Patent 5,742,168).

In view of the above amendments and these remarks, reconsideration of the above noted rejections and objections is respectfully requested.

Rejections under 35 USC 102(b):

Applicant respectfully traverses the rejection of **claims 1-7, 9-11 and 18-20** under 35 USC 102(b) as being anticipated by *Maeng, et al.* The independent claims are **1, 7, 9 and 18**. Each of the independent claims, as amended above, calls for "only one" IC package mounted on each PCB. (**Claim 1**, lines 3-7; **Claim 7**, lines 3-4; **Claim 9**, lines 3-4; and **Claim 18**, lines 3-5.) Applicant respectfully submits that *Maeng, et al.* does not teach or suggest this limitation and other related limitations explained below.

Maeng, et al. describes **several methods** for testing IC chips:

A first method is the prior art in *Maeng, et al.* wherein individual singulated CSPs are inserted into sockets on the burn-in board. (Column 6, lines 25-27) Since the CSPs are inserted directly into the sockets on the burn-in board, this method does not involve the "PCBs," or any other limitations involving the PCBs called for in the claims. (See the limitations in **claim 1**, lines 3-9 and 15; **claim 7**, lines 3-6 and 11-12; **claim 9**, lines 3-9; and **claim 18**, lines 3-7 and 9-13.)

A second method in *Maeng, et al.* is an electric die sorting (EDS) process performed on a plurality of chips that have not yet been cut from a wafer. This process screens out bad chips with failing electrical characteristics. (Column 5, lines 6-12) Since the method is performed on IC chips on an uncut wafer, this method

does not involve "IC packages," or any other limitations involving IC packages, as called for in the claims. (See the limitations in **claim 1**, every limitation; **claim 7**, lines 1-3 and 5-14; **claim 9**, lines 1-4 and 7-11; and **claim 18**, lines 1-5 and 9-13.)

A third method involves forming a "CSP strip" with a plurality of CSPs thereon. (Column 5, lines 22-26; Column 7, lines 2-4) Thus, the CSPs are electrically tested in groups of a CSP strip rather than in groups of individual singulated CSPs. (Column 5, lines 45-47) Since there are a plurality of the CSPs on the CSP strips, this method does not have "only one" IC package on a PCB as called for in the claims. (**Claim 1**, lines 3-7; **Claim 7**, lines 3-4; **Claim 9**, lines 3-4; and **Claim 18**, lines 3-5.)

A fourth method is a burn-in test involving a plurality of CSPs surface-mounted on a module board inserted into a socket on a burn-in board. (column 6, lines 5-9 and 32) Similar to the third method, since there are a plurality of the CSPs on the module board, this method does not have "only one" IC package on a PCB as called for in the claims. (**Claim 1**, lines 3-7; **Claim 7**, lines 3-4; **Claim 9**, lines 3-4; and **Claim 18**, lines 3-5.)

As a consequence, neither the **third method** nor the **fourth method** enables the ability to remove only one module board (claimed PCB) from the burn-in board (claimed motherboard) and perform a test on "only" one CSP (claimed subject IC package) to determine a location of a failure in the CSP as called for in amended **claim 1**, lines 15-17. Similarly, neither the **third method** nor the **fourth method** enables the ability to perform a test on "individual" IC packages on removed PCBs to determine a location of a failure condition as called for in amended **claim 7**, lines 14-15. Furthermore, neither the **third method** nor the **fourth method** enables the ability to test "individual" IC packages to determine whether any of the IC packages failed due to application of a test electrical bias as called for in amended **claim 9**, lines 10-11, and amended **claim 18**, lines 11-13.

Applicant respectfully submits, therefore, that the amended independent **claims 1, 7, 9 and 18** are not anticipated by, are not obvious from, and are

patentable over *Maeng, et al.*, since the reference does not teach or fairly suggest the limitation of having only one IC package mounted on each PCB and, thus, cannot test only one individual IC package at a time. These limitations further enable the ability to narrow down, or fine tune, the location of a failure, as explained in paragraphs [0008] and [0032] of the present specification. On the other hand, having a plurality of the CSPs on the module boards, as described in *Maeng, et al.*, is similar to the problem described in the background of the present specification (paragraphs [0008]-[0009]) wherein it is explained that the IC packages 100 must be "cut" from the PCB 102 in order to perform the manual test that gives a "finer" result.

Additionally, Applicant respectfully submits that, since dependent **claims 1-6, 10-11 and 19-20** depend directly or indirectly from amended independent claims 1, 7, 9 and 18, these claims also are not anticipated by, are not obvious from, and are patentable over *Maeng, et al.* for the same reasons.

Rejections under 35 USC 103(a):

Applicant respectfully traverses the rejection of **claims 8 and 12-17** under 35 USC 103(a) as being unpatentable over *Maeng, et al.*, in view of *Kiyokawa, et al.*

Claims 8 and 12 depend from amended independent claims 7 and 9, respectively. As explained above, amended independent claims 7 and 9 are not anticipated by, are not obvious from, and are patentable over *Maeng, et al.*, since the reference does not teach or fairly suggest the limitation of having only one IC package mounted on each PCB and, thus, cannot test only one individual IC package at a time. Applicant respectfully submits that *Kiyokawa, et al.* does not cure these deficiencies in *Maeng, et al.* Therefore, Applicant respectfully submits that **claims 8 and 12** are not anticipated by, are not obvious from, and are patentable over *Maeng, et al.*, in view of *Kiyokawa, et al.*, since the references do not teach or fairly suggest the limitation of having only one IC package mounted on each PCB and, thus, cannot test only one individual IC package at a time.

Claim 13 is independent and has been amended above. **Claims 14-17** depend from amended independent claim 13. **Claim 13**, as amended above, calls

for "only one" IC package mounted on each PCB. (**Claim 13**, lines 3-4.) Applicant respectfully submits that *Maeng, et al.* does not teach or suggest this limitation and other related limitations as explained above with respect to the 102(b) rejections. Additionally, Applicant respectfully submits that *Kiyokawa, et al.* does not cure these deficiencies in *Maeng, et al.* Therefore, Applicant respectfully submits that amended independent **claim 13** is not anticipated by, is not obvious from, and is patentable over *Maeng, et al.*, in view of *Kiyokawa, et al.*, since the references do not teach or fairly suggest the limitation of having only one IC package mounted on each PCB and, thus, cannot test only one individual IC package at a time, as called for in amended independent **Claim 13**, lines 3-4 and lines 12-14. Additionally, Applicant respectfully submits that, since dependent **claims 14-17** depend directly or indirectly from amended independent claim 13, these claims also are not anticipated by, are not obvious from, and are patentable over *Maeng, et al.* in view of *Kiyokawa, et al.* for the same reasons.

For the reasons specifically discussed above, and others, it is believed that pending **claims 1-20** define patentable subject matter. Reconsideration of the previous rejections as they might apply to the pending claims is therefore respectfully requested. Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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